Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTONS:**

1. **–IN A**
2. **+IN A**
3. **OFFSET A**
4. **V-**
5. **OFFSET B**
6. **+IN B**
7. **–IN B**
8. **OFFSET B**
9. **V+ (B)**
10. **OUTPUT B**
11. **N.C.**
12. **OUTPUT A**
13. **V+ (A)**
14. **OFFSET A**

**12 11 10**

**13**

**14**

**1**

**2**

**9**

**8**

**7**

**6**

**3 4 5**

**MASK**

**REF**

**N**

**S**

**C**

**7**

**4**

**7**

**D**

**.064”**

**.079”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential:**

**Mask Ref: NSC747D**

**APPROVED BY: DK DIE SIZE .064” X .079” DATE: 7/7/22**

**MFG: NATIONAL THICKNESS .010” P/N: LM747**

**DG 10.1.2**

#### Rev B, 7/19/02